Full Listing of the Claims (NO Amendments)

Please amend the claims in the manner indicated.

1. (previously presented) A method comprising:

detecting an electrical characteristic identifying a defect in a memory unit; and

replacing the memory unit with an alternate memory unit, wherein the replacing is performed during user operation of a device having the memory unit and the alternate memory unit;

wherein the detecting is performed during an erase operation.

2. (original) The method as recited in Claim 1, wherein the detecting the electrical characteristic comprises:

monitoring a current during an erase attempt; and

identifying the defect when the current passes a predetermined current threshold.

3. (original) The method as recited in Claim 1, wherein the detecting the electrical characteristic comprises:

monitoring a voltage during an erase attempt; and

identifying the defect when the voltage passes a predetermined voltage threshold.

4. (original) The method as recited in Claim 1, wherein the detecting the electrical characteristic comprises:

monitoring a resistance during an erase attempt; and

identifying the defect when the resistance passes a predetermined resistance threshold.

5. (canceled)

6. (original) The method as recited in Claim 1, wherein the replacing the memory unit with the alternate memory unit comprises:

causing the memory unit to be un-accessible at a memory address; and

causing the alternate memory unit to be accessible at the memory address.

7. (original) The method as recited in Claim 6, wherein the causing the alternate memory unit to be accessible comprises:

programming address status bits of the alternate memory unit with the memory address.

8. (original) The method as recited in Claim 7, wherein the address status bits comprise non-volatile memory.

9. (original) The method as recited in Claim 7, wherein the address status bits comprise programmable fuses.

10. (original) The method as recited in Claim 6, wherein the causing the alternate memory unit to be accessible comprises:

setting a used status bit of the alternate memory unit.

11. (original) The method as recited in Claim 1, wherein the memory unit is a flash memory block.

12. (original) The method as recited in Claim 1, wherein the memory unit is a row of flash memory.

13. (original) The method as recited in Claim 1, wherein the memory unit is a row of polymer memory.

14. (previously presented) An apparatus comprising:

a plurality of accessible memory units;

one or more redundant memory units;

a failure detection unit coupled to the plurality of accessible memory units configured to monitor electrical characteristics in the plurality of accessible memory units during an erase operation and detect an electrical characteristic that identifies a defect in one of the plurality of accessible memory units; and

a redundant block swap unit coupled to the plurality of accessible memory units and the one or more redundant memory units, the redundant block swap unit configured to replace the one of the plurality of accessible memory units with one of the one or more redundant memory units.

15. (previously presented) The apparatus as recited in Claim 14, the failure detection circuit comprising:

a current detection unit to detect a current during the erase operation.

16. (previously presented) The apparatus as recited in Claim 14, the failure detection circuit comprising:

a voltage detection unit to detect a voltage during the erase operation.

17. (previously presented) The apparatus as recited in Claim 14, the failure detection circuit comprising:

a resistance detection unit to detect a resistance during the erase operation.

18. (original) The apparatus as recited in Claim 14, wherein each of the one or more redundant memory units comprises:

a plurality of memory cells;

address status bits; and

a used status bit;

wherein the redundant block swap unit is configured to program the address status bits and the used status bit to cause the plurality of memory cells to be accessible.

19. (original) The apparatus as recited in Claim 14, wherein each of the one or more redundant memory units comprises a plurality of memory cells, the apparatus further comprising:

address status bits; and

a used status bit;

wherein the redundant block swap unit is configured to program the address status bits and the used status bit to cause the plurality of memory cells to be accessible.

20. (original) A system comprising:

a processor;

an antenna coupled to the processor; and

a memory device coupled to the processor, the memory device comprising:

a plurality of accessible memory units;

one or more redundant memory units;

a failure detection unit coupled to the plurality of accessible memory units configured to monitor electrical characteristics in the plurality of accessible memory units and to detect a electrical characteristic that identifies a defect in one of the plurality of accessible memory units; and

a redundant block swap unit coupled to the accessible memory units and the one or more redundant memory units, the redundant block swap unit configured to replace the one of the plurality of accessible memory units with one of the one or more redundant memory units.

21. (original) The system as recited in Claim 20, the failure detection circuit comprising:

a current detection unit to detect a current in one of the plurality of accessible memory units during an erase operation.

22. (original) The system as recited in Claim 21, wherein each of the one or more redundant memory units comprises:

a plurality of memory cells;

address status bits; and

a used status bit;

wherein the redundant block swap unit is configured to program the address status bits and the used status bit to cause the plurality of memory cells to be accessible.

23. (original) The system as recited in Claim 20, wherein each of the one or more redundant memory units comprises a plurality of memory cells, the memory device further comprising:

address status bits; and

a used status bit;

wherein the redundant block swap unit is configured to program the address status bits and the used status bit to cause the plurality of memory cells to be accessible.

24. (previously presented) An apparatus comprising:

a computer readable medium; and

instructions stored on the computer readable medium to:

detect an electrical characteristic that identifies a defect in a memory unit; and

replace the memory unit with an alternate memory unit, wherein replacing is performed during user operation of a device having the memory unit and the alternate memory unit;

wherein the electrical characteristic is detected during an erase operation.

25. (original) The apparatus as recited in Claim 24, wherein the instructions to detect the electrical characteristic comprises instructions to:

monitor a current; and

identify a defect when the current exceeds a predetermined current threshold.

26. (original) The apparatus as recited in Claim 24, wherein the instructions to detect the electrical characteristic comprises instructions to:

monitor a voltage during an erase attempt; and

identify a defect when the voltage exceeds a predetermined voltage threshold.

27. (canceled)

28. (original) The apparatus as recited in Claim 24, wherein the instructions to replace the memory unit with an alternate memory unit comprises instructions to:

cause the memory unit to be un-accessible at a memory address; and

cause the alternate memory unit to be accessible at the memory address.

29. (original) The apparatus as recited in Claim 28, wherein the instructions to cause the alternate memory unit to be accessible comprises instructions to:

program address status bits of the alternate memory unit with the memory address.

30. (original) The apparatus as recited in Claim 28, wherein the instructions to cause the alternate memory unit to be accessible comprises instructions to:

set a used status bit of the alternate memory unit.

31. (original) The apparatus as recited in Claim 24, wherein the memory unit is a flash block.